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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,164	10/31/2003	Tae Young Lim	123034-05004771	6449

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EXAMINER	
WANG, BEN C	
ART UNIT	PAPER NUMBER
2196	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,164	LIM ET AL.	
	Examiner	Art Unit	
	Ben C. Wang	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :09/18/2006,05/11/2006, 10/31/2003.

DETAILED ACTION

1. Claims 1-16 are pending in this application and presented for examination.

Claim Objections

2. Claims 16 is objected to because the following informalities:

"verifying procedures by a 6CAD tool.", claim 16, line 4, should be corrected as

"verifying procedures by a CAD tool".

Appropriate correction is required.

Claim Rejections – 35 USC § 103(a)

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-5, 7, 9, 12-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pochayevets et al. (hereafter 'Pochayevets') (Pub. No. US 2004/0019873 A1) in view of Dalton Project (hereafter 'Dalton') (http://www.cs.ucr.edu/~dalton/i8051/i8051syn - Synthesizable VHDL Model of 8051/testall.hex and Simulation, 02/20/2001, Dept. of Computer Science, University of California).

5. **As to claim 1**, Pochayevets discloses a method of creating a ROM soft IP ([0070]) comprising the steps of: (a) preparing a head file which describes the initial information of the ROM soft IP in a given electronic circuit design language ([0003]; [0004], Lines 1-7 (entity); [0007], Lines 1-4; 1-8 (architecture); [0013], Lines 1-8 (configuration); [0018], Lines 1-6, 9-12; an exemplary head file is shown in Fig. 3, from LIBRARY IEEE statement to BEGIN statement), a tail file which describes the end information of the ROM soft IP in the given electronic circuit language (an exemplary tail file is shown in Fig. 3, END struct statement), and an empty ROM soft IP file ([0018], Lines 3-6).

Pochayevets does not specifically disclose a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters and hex data structure and converting the hex file for the MPU program memory into the given electronic circuit design language expression and selecting a hex file for an MPU program memory and (b) copying the head file into the first part of the empty ROM soft IP file, and writing the converted expression into the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file.

However, in an analogous art, Dalton discloses a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters (testall.hex and other hex test files) and converting the hex file for the MPU program memory into the given electronic circuit design language expression (*Synopsys Simulation for Beginners*, Sec. 3 (Simulate), Step 1, Lines 1 - converting your C file to VHDL ROM model, 3 – compile your C file into Intel hex format, 8 – Convert your hex file into a VHDL ROM model, and

11 – a file called i8051_rom.vhd will be generated; See i8051_rom.vhd file content listing) and selecting a hex file for an MPU program memory (*Synopsys Simulation for Beginners*, Sec. 3 (Simulate), Step 1, bullet 2 – convert your hexfile into a VHDL ROM model) and (b) copying the head file into the first part of the empty ROM soft IP file, and writing the converted expression into the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file (*Synopsys Simulation for Beginners,* Sec. 3 (Simulate), bullet 2, 3rd step – i8051_rom.vhd will be generated; i8051_rom.vhd file content -- it includes head-part, middle-part, and tail part. All parts are written in VHDL).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and the teachings of Dalton to further provide a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters and converting the hex file for the MPU program memory into the given electronic circuit design language expression in Pochayevets system.

The motivation is to provide an alternative way for the hex data generation and its associated VHDL conversion process for ROM SoftIP generator model.

6. **As to claim 9**, Pochayevets discloses a computer readable recording media having a program for executing a method of creating a ROM soft IP ([0070]) the steps of: (a) preparing a head file which describes the initial information of the ROM soft IP in a given electronic circuit design language ([0003]; [0004], Lines 1-7 (entity); [0007],

Lines 1-4; 1-8 (architecture); [0013], Lines 1-8 (configuration); [0018], Lines 1-6, 9-12; an exemplary head file is shown in Fig. 3, from LIBRARY IEEE statement to BEGIN statement), a tail file which describes the end information of the ROM soft IP in the given electronic circuit language (an exemplary tail file is shown in Fig. 3, END struct statement), and an empty ROM soft IP file ([0018], Lines 3-6).

Pochayevets does not specifically disclose a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters and hex data structure and converting the hex file for the MPU program memory into the given electronic circuit design language expression and selecting a hex file for an MPU program memory and (b) copying the head file into the first part of the empty ROM soft IP file, and writing the converted expression into the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file.

However, in an analogous art, Dalton discloses a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters (testall.hex and other hex test files) and converting the hex file for the MPU program memory into the given electronic circuit design language expression (Page 2, Sec. 3, Step 1, Lines 1 - converting your C file to VHDL ROM model, 3 – compile your C file into Intel hex format, 8 – Convert your hex file into a VHDL ROM model, and 11 – a file called i8051_rom.vhd will be generated; See i8051_rom.vhd file content listing) and selecting a hex file for an MPU program memory (*Synopsys Simulation for Beginners*, Sec. 3 (Simulate), Step 1, bullet 2 – convert your hexfile into a VHDL ROM model) and (b) copying the head file into the first part of the empty ROM soft IP file, and writing the converted expression into

the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file (*Synopsys Simulation for Beginners*, Sec. 3 (Simulate), bullet 2, 3rd step – i8051_rom.vhd will be generated; i8051_rom.vhd file content – it includes head-part, middle-part, and tail part. All parts are written in VHDL).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and the teachings of Dalton to further provide a hex file, which includes a start address (s) and an instruction (s) composed of ASCII characters and converting the hex file for the MPU program memory into the given electronic circuit design language expression in Pochayevets system.

The motivation is to provide an alternative way for the hex data generation and its associated VHDL conversion process for ROM SoftIP generator model.

7. **As to claims 4 and 12**, Pochayevets discloses the ROM soft IP can be built in the MPU instead of a mask ROM ([0068]).

8. **As to claim 5 and 13**, Pochayevets discloses the head file has the initial information including a library ([0072], rom.vhd listing, LIBRARY IEEE) to be applied to the IP, the name of the IP ([0072], rom.vhd listing, ENTITY rom IS), and an input/output signal ([0072], rom.vhd listing, PORT(in_adr: IN ....; out_d: OUT ....), and the statement for describing the ROM address ([0072], rom.vhd listing, run: PROCESS(in_adr)) and the instruction at the address ([0072], rom.vhd listing, for example, out_d <=

"01111101100010100101111100111110";) the initial information and the statement being described in the electronic circuit design language ([0072], rom.vhd listing), and the tail file has last data of the ROM and an end statement described in the electronic circuit design language ([0072], rom.vhd, ELSIF in_adr = "11" THEN out-d <= "01000111000111001110110011100110"; END IF; END PROCESS run; END str;).

9. **As to claims 7 and 15**, Pochayevets discloses the ROM soft IP described in the electronic circuit design language is incorporated with an MPU core IP and is built-in as an accessory ([0020], Lines 1-3; [0024], Lines 8-9; [0025]; [0026]; [0027]; [0028]; Fig. 15; [0070]).

10. Claims 3, 8, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pochayevets in view of Dalton and further in view of S. Meyer (hereafter 'Meyer') (Pub. No. US 2002/0138244 A1).

11. **As to claims 3 and 11**, Pochayevets discloses creating the ROM soft IP wherein the ROM soft IP is described in any one of the electronic circuit design languages including very high speed description language (VHDL) (Fig. 15; [0085]).

Pochayevets and Dalton do not disclose the ROM soft IP is described in Verilog.

However, in an analogous art, Meyer discloses creating the ROM soft IP ([0096], Lines 1-5) wherein the ROM soft IP is described in Verilog (Fig. 1; [0015], Lines 1-2, 4-5).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and Dalton with the teachings of Meyer to create the ROM soft IP wherein the ROM soft IP is described in Verilog in Pochayevets-Dalton system.

The motivation is to further expand HDL Soft IP creation method to include Verilog to provide wider choices for customers.

12. **As to claims 8 and 16**, Pochayevets and Dalton do not disclose creating the ROM soft IP further comprising the step of incorporating the ROM soft IP with the MPU core IP and performing circuit synthesizing and verifying procedures by a CAD tool.

However, in an analogous art, Meyer discloses creating the ROM soft IP further comprising the step of incorporating the ROM soft IP with the MPU core IP and performing circuit synthesizing and verifying procedures by a CAD tool ([0003], Lines 1-4, 11-13).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and Dalton with the teachings of Meyer to create the ROM soft IP by incorporating the ROM soft IP with the MPU core IP and performing circuit synthesizing and verifying procedures by a CAD tool in Pochayevets-Dalton system.

The motivation is to further provide an integrated tool set to perform circuit synthesizing, simulation and verification.

13. Claims 2, 6, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pochayevets in view of Dalton and further in view of D. Wallner (hereafter 'Wallner') (http://www.opencores.org/cvsweb.shtml/ax8/sw/hex2rom.cpp - Revision 1.4, 10/27/2002, OPENCORES.ORG).

14. **As to claims 2 and 10**, Pochayevets and Dalton do not disclose creating the ROM soft IP wherein the procedure of converting the hex file for the MPU program memory into the given electronic circuit design language expression in the step (b) is performed by analyzing the start address (s) and the instruction (s) in the hex file and transforming them into binary codes, respectively.

However, in an analogous art, Wallner discloses creating the ROM soft IP wherein the procedure of converting the hex file (P. 11, inFile.ReadHex(...) – *called from the main program*, P. 3, void ReadHex(...)) for the MPU program memory into the given electronic circuit design language expression (P. 12, i.e., library IEEE contained in printf("\nlibrary IEEE;");) in the step (b) is performed by analyzing the start address (s) (P. 4, if (sscanf(&szLine[1], "%2lx%4lx%2lx", &dataBytes, &startAddress,....)) and the instruction (s) in the hex file (P.3, while (!feof(m_file)...) and transforming them into binary codes (P.13, inFile.BitString(...)), respectively.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and Dalton with the teachings of Wallner to create the ROM soft IP wherein the procedure of converting the hex file for the MPU program memory into the given electronic circuit design

language expression in the step (b) is performed by analyzing the start address (s) and the instruction (s) in the hex file and transforming them into binary codes, respectively in Pochayevets-Dalton system.

The motivation is to further obtain the ROM specified configuration information to convert hex-decimal input file into a VHDL ROM target model.

15. **As to claims 6 and 14**, Pochayevets and Dalton do not disclose creating the ROM soft IP wherein the procedure of converting the instruction into the electronic circuit design language in the step (b) is performed by describing the number of the instructions of the hex file composed of ASCII characters in a decimal by using a function converting a character into an integer.

However, in an analogous art, Wallner discloses creating the ROM soft IP wherein the procedure of converting the instruction into the electronic circuit design language in the step (b) is performed by describing the number of the instructions of the hex file composed of ASCII characters in a decimal by using a function converting a character into an integer (P. 3, char szLine[1024] – *a character-array*; P. 4, unsigned long tmp – *an unsigned integer*; if (sscanf(&szLine[1], "%2lx%4lx%2lx", &dataBytes, &startAddress,....) – dataBytes – *it contains how many bytes of data (instructions)*; convert szLine[.] (char) into tmp (unsigned long) – *it means converting a character (one-byte) into an unsigned integer (four-byte, for example)*).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Pochayevets and Dalton with

the teachings of Wallner to create the ROM soft IP wherein the procedure of converting the instruction into the electronic circuit design language in the step (b) is performed by describing the number of the instructions of the hex file composed of ASCII characters in a decimal by using a function converting a character into an integer in Pochayevets-Dalton system.

The motivation is to further obtain more detained ROM configuration data to configure and to debug Soft IP generator.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

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BCW BW

December 13, 2006

N. El-Hady

NABIL M. EL-HADY
SUPERVISORY PATENT EXAMINER